Design and Performance of Octave *S/C*-Band MMIC T/R Modules for Multi-Function Phased Arrays

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Abstract—**A complex wideband transmit/receive module that has achieved performance levels superior to any MMIC module will be described. Peak performance within the octave 3.0 to 6.0 GHz band includes a power output of 21 W at *S*-band and 19 at *C*-band, a noise figure of 3.9 to 5.0 dB, 30 to 38 dB of receive gain, 25 to 26 dBm output IP_3, 40 dB of gain control in 256 steps, dual receive channels with independent amplitude and phase control, and an 8-bit phase shifter with less than 1 degree calibrated rms phase error. Total GaAs area is 146 mm^2 with 170 mm of total gate periphery. The module incorporates a compact digital interface, requires only three supply voltages, and utilizes advanced packaging techniques, resulting in a size compatible with a grating lobe free grid spacing.**

Introduction

MMIC's have the ability to enable new system concepts that could not be brought to fruition without this technology, hence the recent intensity of development activity surrounding the electronically-scanned phased array. Since many potential applications contain functions that can be reduced to a generic set of requirements, wideband components have frequently been the focus of development. The MMIC's and the T/R modules described here were specifically designed for wideband operation, providing continuous octave band coverage from 3.0 to 6.0 GHz.

Architecture

In order to maximize performance and minimize the cost of this module a shared leg architecture shown in Fig. 1 was selected. The shared leg, used for both transmit and receive, includes a variable gain amplifier, phase shifter, and gain blocks. Connection to either the final output amplifiers on transmit or the LNA on receive is accomplished through the use of a DPDT transfer switch. There are several advantages to this architecture over the conventional bidirectional phase shifter approach: 1) it minimizes the number of components since gain stages are shared between transmit and receive; 2) the receive dynamic range is maximized since gain stages can be distributed before and after the "lossy" phase shifter; 3) the VGA can be used for programmable transmit aperture tapering as well as on receive; 4) the shared leg can be designed as an integrated chip using a versatile high yield MMIC process without degrading module performance specifications. Separate HPA and LNA devices optimized for the specific band of operation insure that advances in device technology of these components, such as HBT and HEMT, can be incorporated with minimal impact.

Independent Receive Channels

Independent phase and amplitude control channels are implemented on receive. This implementation circumvents many of the difficulties in achieving phase and amplitude tracking between the three complex beamforming networks required of a monopulse radar [1], [2]. If only a single receive channel existed, only the sum channel could be corrected. Since the amplitude and phase errors of the difference channel are generally uncorrelated and larger than the sum channel (180-degree hybrids must be employed rather than in-phase Wilkinsons), the achievable difference beam sidelobe level is higher. With the two receive channel module configuration, the beamformers are greatly simplified. There is no need to form sums and differences from subarrays equidistant from the array centerline, and hence the expense, size, and weight associated with phase-tracked RF cabling has been eliminated. Similarly, difference hybrids have been eliminated, as an extra 180 degree phase shift can be added in the module. Finally, errors in amplitude and phase can be corrected at each frequency to maintain low sidelobes, an extremely important factor since we are dealing with a wideband octave system rather than a narrowband requirement.

Architecture Implications

The requirements placed on the MMIC's described subsequently are directly descended from the chosen architecture and the system application, but deserve discussion here. Both 8-bits of amplitude and phase control

Manuscript received March 21, 1991; revised June 27, 1991.

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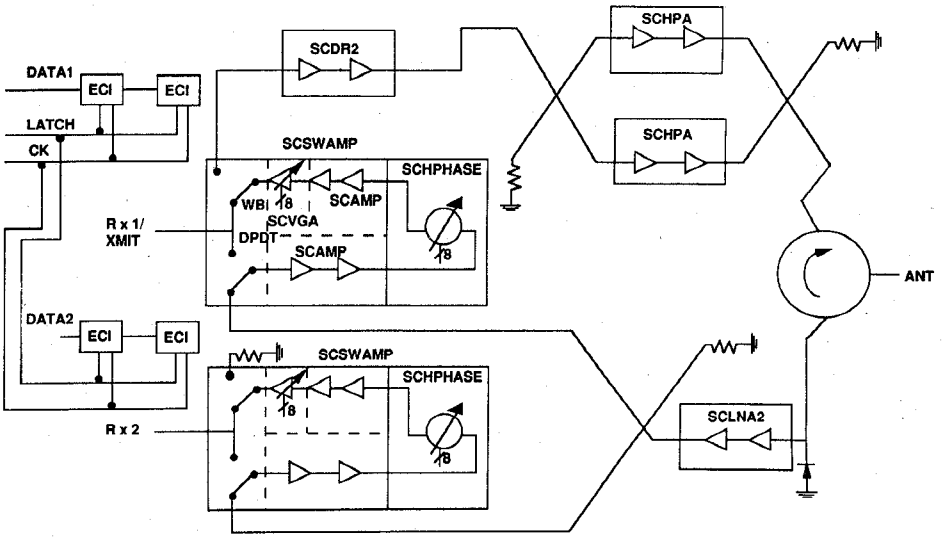


Fig. 1. Block diagram of S/C-band T/R module.

have been selected, although less than 30 dB of amplitude range and six-bit accuracy are required by most applications. The philosophy here is one of tolerance funneling to guarantee a low-cost module in manufacturing. The extra bits allow tolerance for finite RF performance distributions of the MMIC's, without paying a resolution/adjustment range penalty for module-to-module tracking or requiring module tuning. Secondly, the shared leg architecture places additional constraints on the circuit design. In particular, any leakage signal from the input to output path will corrupt the response and produce amplitude/phase ripple across frequency. In the ultimate case, if the variable gain amplifier is not placed last, for large gain reductions, the leakage path may actually dominate and phase control may be lost. Placing the VGA last however, requires that the device be capable of a power output commensurate with low IMD products (intermodulation distortion). Leakage can also occur due to bulk GaAs substrate/dielectric mode propagation, common bias networks, and finite transfer switch isolation. Substrate modes are effectively suppressed by careful layout to provide a picket fence of ground vias through the center of the chip. Bias networks should be extensively reactively and *RC* filter decoupled, and switch isolation is obtained by careful multi-stage series/shunt switch design.

MMIC Chip Set

The module described subsequently is composed of a dozen chips of six types, HPA, driver, LNA, switch/amplifier, phase shifter, and interface. Of these the switch/amplifier and phase shifter constitute the shared leg which is used twice in the dual receive channel configuration. This shared leg has been partitioned into an RF-testable two chip set due to cost/yield considerations, an 8-bit phase shifter (SCPHASE), and an integrated "super-chip" incorporating a DPDT transfer switch, an 8-bit variable gain amplifier, and four stages of gain blocks (SCSWAMP).

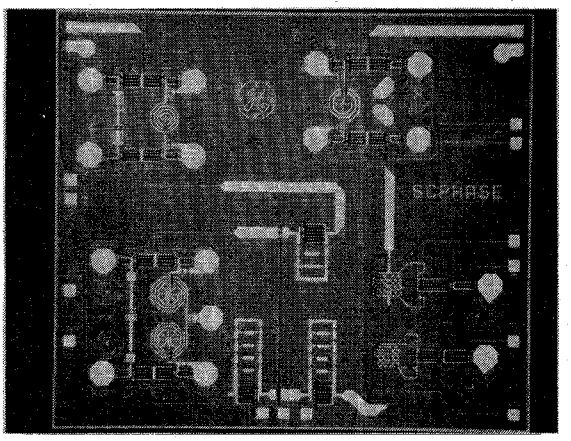


Fig. 2. Phase shifter MMIC (SCPHASE).

Phase Shifter

The wafer-probeable phase shifter, shown in Fig. 2, is based on an extensive effort at GE in researching and optimizing phase shifter topology for not only RF performance, but process insensitivity and high yield [3], [4]. The electrical parameters considered are phase ripple, insertion loss, the difference in insertion loss between states, VSWR, and the circuit element values required. Phase ripple and insertion loss between states are important because they impact the complexity of the calibration scheme. A good VSWR is required to minimize interaction between bits as well as between MMIC's. Insertion loss is slightly less important due to the shared leg architecture, i.e., gain can be made up by active elements without degrading IMD or noise figure. Some circuit approaches can be rejected because the circuit element values required are unrealizable due to parasitic effects.

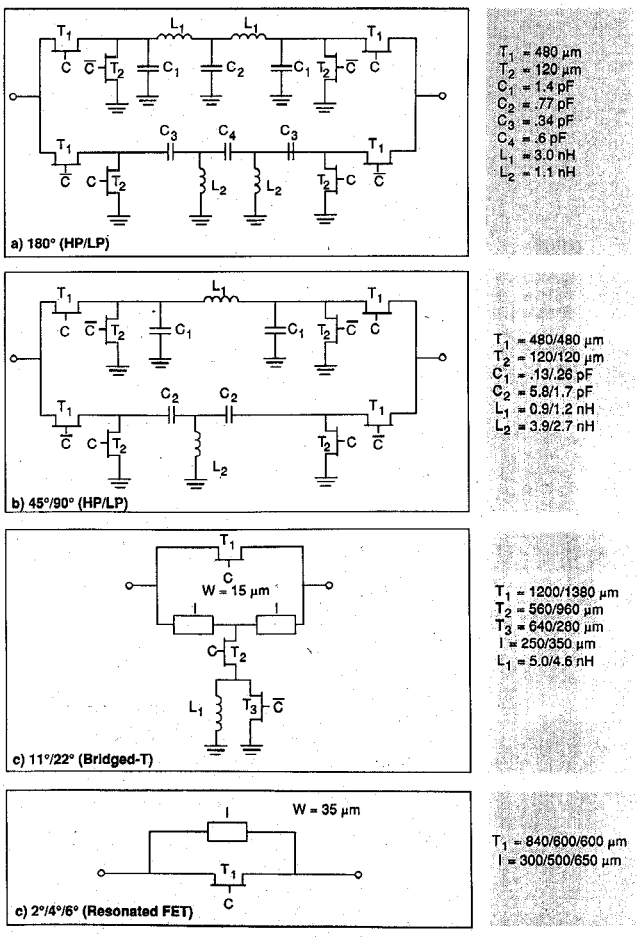


Fig. 3. Schematics of individual phase bits.

Cost and yield limiting factors considered are chip size, total MESFET periphery, and process sensitivity. The cost of processing a wafer is relatively constant given a certain level of automation, so the more circuits per wafer, the lower the cost of the chip. Visual and dc yields seem to be weakly dependent on chip size and MESFET periphery. Slight variations in material and processing will cause a spread in RF circuit performance. Design centering will thus maximize yield, but it is also necessary to minimize the standard of deviation of RF performance by selecting phase shifter topologies that will minimize the process sensitivity factor.

The chosen lumped element topologies, shown in Fig. 3, have successfully realized both narrowband (L, C, X) and wideband (3-6 GHz, 3–11 GHz) designs. The 180, 90, and 45 degree bits are FET-switched high-pass/low-pass structures, the 22 and 11 degree bits are FET-switched bridged T's, while the three LSB's are resonated FET's. The FET-switched high-pass/low-pass bits employ a series/shunt SPDT switch configuration (T_1 and T_2 in Fig. 3(a) and (b)) to select the proper filter. The high-pass and low-pass filters are realized with lumped elements, MIM capacitors and spiral inductors. The 180° bit uses five section filters, while the 45° and 90° bits use three section filters. For the FET-switched bridged T configuration, the switching FET's are integrated into high-pass/low-pass T filters. The high pass circuit is formed by a spiral inductor (L_1 in Figure 3(c)) with T_1 and T_2 biased on and T_3 biased off), while the low-pass circuit is formed by two inductive lengths of transmission line (l in Fig. 3(c)) and the "off" capacitance of one of the switching FET's (T_2 in Fig. 3(c)). The inductors (L_1 and l in Fig. 3(c)), and two of the switching FET's (T_2 and T_3 in Fig. 3(c)) are sized for proper phase shift, and one of the switching FET's (T_1 in Fig. 3c) is sized for insertion loss balance between states. In the resonated FET configuration, the switching FET is parallel resonated with an inductor, realized with high impedance microstrip (l in Fig. 3(d)). The FET periphery (T_1 in Fig. 3(d)) is selected to give equal insertion loss for both phase states, and the inductance is selected to give the desired phase shift. Chip size is 3.8 mm×3.3 mm, while typical performance across the 256 phase states is 10 dB insertion loss, ±1.0 dB maximum amplitude variation with less than 1 degree calibrated rms phase error. The input power at one dB compression is +22 dBm.

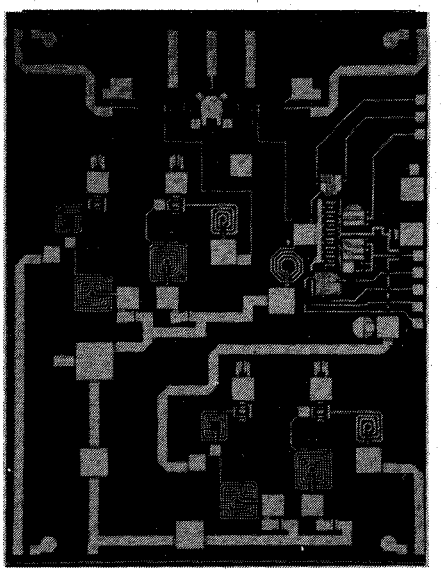
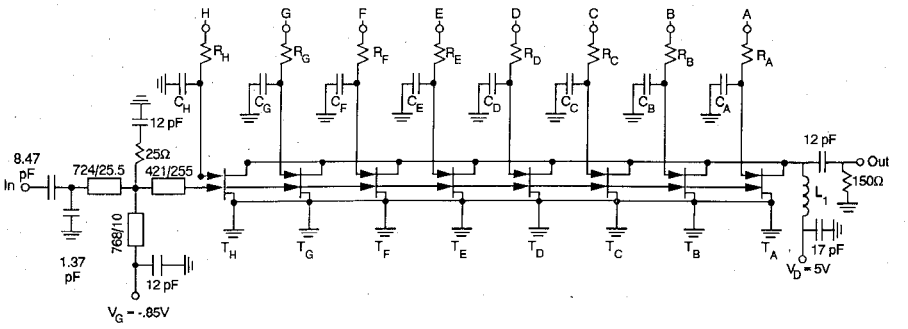


Fig. 4. Switch/amplifier MMIC (SCSWAMP).

Switch / Amplifier

The SCSWAMP "super-chip," shown in Fig. 4, is a wafer-probeable MMIC incorporating a transfer switch, gain blocks, and a variable gain amplifier.

The DPDT transfer switch is a wideband dc-18 GHz design using series and shunt FET's as switching elements. The switching FET appears as a low series resistance in the "ON" state, and a series resistance/capacitance in the "OFF" state. The switch configuration utilizes a pair of series/shunt switches in the beamformer port, and a pair of series switches for routing signals at the LNA/IN and PA/OUT junctions. Inductance, realized as high impedance microstrip, is employed to resonate out the capacitive component of the "OFF" state FET's. Typical performance of the switch is less than 2 dB



T_A	= 800 μm (8 x 100)	R_A	= 100Ω x 4	C_A	= 2.5 pF x 4
T_B	= 400 μm (4 x 100)	R_B	= 100Ω x 2	C_B	= 2.5 pF x 2
T_C	= 200 μm (2 x 100)	R_C	= 100Ω x 1	C_C	= 2.5 pF x 1
T_D	= 100 μm (1 x 100)	R_D	= 200Ω	C_D	= 1.25 pF
T_E	= 50 μm	R_E	= 400Ω	C_E	= .625 pF
T_F	= 25 μm	R_F	= 800Ω	C_F	= .312 pF
T_G	= 12.5 μm	R_G	= 1600Ω	C_G	= .156 pF
T_H	= 6.25 μm	R_H	= 3200Ω	C_H	= .078 pF
L_1	= 2.0 nH				

Fig. 5. Schematic of segmented dual gate VGA.

insertion loss per pole with better than 30 dB isolation through 18 GHz.

The variable gain amplifier, shown schematically in Fig. 5, is based upon the segmented dual gate FET approach [5], [6]. Conventionally, dual gate MESFET's have been used for gain control by applying an analog voltage to gate #2. The control is nonlinear and alters device impedances as shown in [5], making it difficult to provide a control voltage with precision and repeatability that does not alter phase while changing gain. In contrast, the segmented dual gate MESFET's (SDGFET's) obtain precise amplitude control with a minimum of incidental phase shift.

In this approach, the second gate of the dual gate MESFET is digitally-controlled to selectively switch ON/OFF portions of the SDGFET total gate periphery in order to achieve a desired state. The ON/OFF control is achieved by switching the gate #2 bias voltage levels between saturation and pinch-off, while the gate #1 voltage is held constant (control points A through H in Fig. 5). The reference maximum gain state of the SDGFET is when all segments of the device are biased on. A specific gain/attenuation level can be selected by turning off portions of the total SDGFET periphery. The gain of the device is proportional to the collective width of the on segments. The device is composed of segments integrated together by connecting the gate #1, source, and drain electrodes. The layout geometry of the segments is the same to preserve linear scaling of electrical parameters.

SDGFET devices are operated in a cascode configuration with the second gate RF grounded via a shunt capacitor (C_A through C_H in Fig. 5), and use resistors (R_A through R_H in Fig. 5) for isolation from the control voltage source. The relative phase shift of the SDGFET between states can be minimized by proper selection of the gate #2 termination capacitors. These capacitors scale in proportion to gate width of a particular segment, since the device impedance scales with gate width of a particular segment. If the segments are scaled in a binary fashion as in this case, ideally a linear voltage gain curve results with 6 dB steps between major bit transition states (such as 10000000 to 01111111). Antenna system analysis has shown that linear voltage scaling achieves a lower rms sidelobe level than the conventionally used dB scaling.

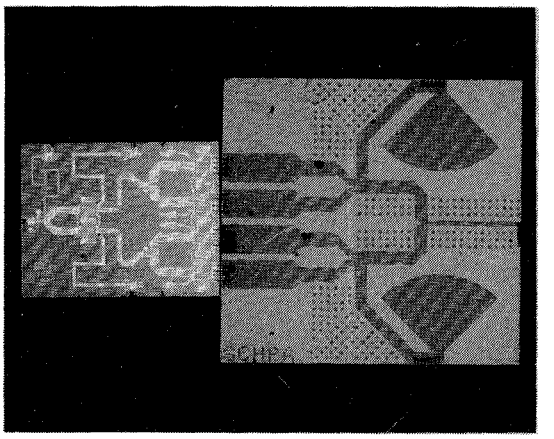


Fig. 6. Power amplifier MMIC (SCHPA).

The gain blocks are based upon a self-biased shunt feedback amplifier for process insensitivity, and flat gain/good VSWR across the 3.0 to 6.0 GHz band. The self-bias arrangement, since it does not require a negative supply, has reduced the gate voltage modulation sensitivity of the module to power supply variation, and as a series feedback mechanism, has reduced temperature variation as well.

Switch/amplifier chip size is 3.8 mm×4.7 mm, while typical performance is 9 dB forward path (switch to phase shifter) and 19 dB reverse path (phase shifter to switch)

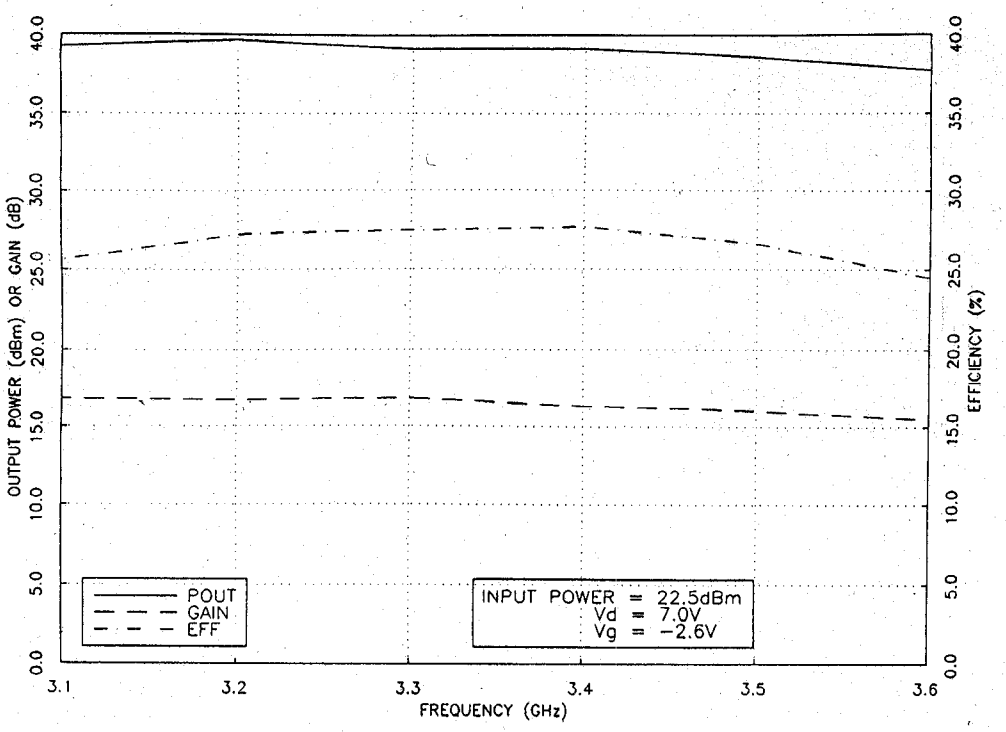


Fig. 7. Class AB performance of SCHPA.

gain, with over 40 dB of gain control range in 256 linear voltage steps. Output third order intercept point ranges from +25 to +26 dBm across 3.0 to 6.0 GHz, while the 1 dB gain compression output power is +16 dBm.

Power Amplifier

The power amplifier shown in Fig. 6, has established a new standard for power output and bandwidth in MMIC form [7]. The amplifier consists of an 8 mm cell divided into two segments, driving four 8 mm cells, resulting in an overall gate periphery of 40 mm. The four output cells are then matched to 50 Ω utilizing an off-chip matching network on 5 mil thick high dielectric constant ($\epsilon_r = 37$) barium titanate material. This approach maximizes power output by reducing output network losses, improves chip cost by improving per wafer yield (smaller MMIC), yet maintains an amplifier envelope commensurate with a totally monolithic implementation. Chip size is 5.8 mm × 4.3 mm, while the output network measures 8.7 mm × 8.2 mm. In Class A operation, typical performance of the power amplifier versus frequency for a constant power input is a power output of 11 ± 1 dB with an associated power gain of 10.5 to 12.5 dB. In Class AB at a lower drain voltage, 9 W at 27% power-added efficiency with 16 dB of power gain is typical at *S*-band as shown in Fig. 7. The test condition for this data was 100 μs pulse width at 10% duty cycle. Additional performance data for other pulse widths and duty cycles can be found in reference [7].

Driver Amplifier

Fig. 8 is the driver amplifier (SCDR2), which like the power amplifier was processed at Harris Microwave Semiconductor using their 0.5 μm P5 implant process. It produces 2 to 4 W with 16 dB power gain from 3.0 to 6.0 GHz. The design consists of a 2.4 mm cell driving four 2.4 mm cells, with a chip size of 4.6 mm × 4.2 mm. Like the power amplifier, the driver utilizes an off-chip matching network on 5 mil high dielectric constant material (4.0 mm × 3.0 mm).

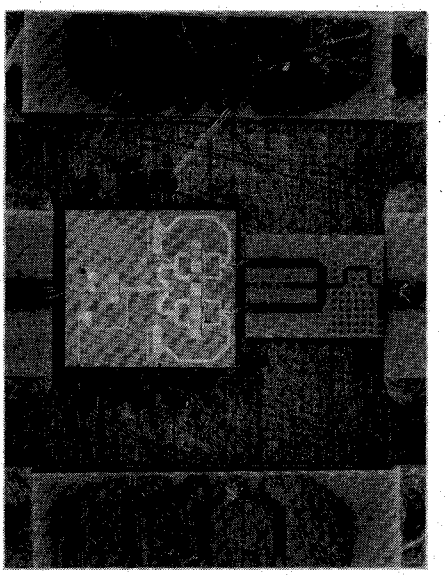


Fig. 8. Driver amplifier MMIC (SCDR2).

Low Noise Amplifier

The two-stage MMIC low noise amplifier (SCLNA2) shown in Fig. 9, has established new benchmarks for wideband noise figure and LNA spur-free dynamic range

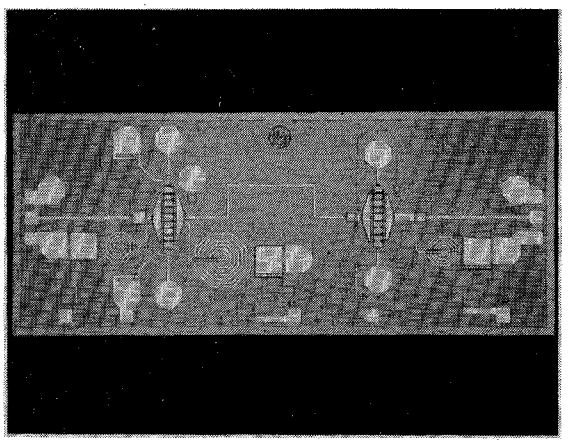


Fig. 9. Low noise amplifier MMIC (SCLNA2).

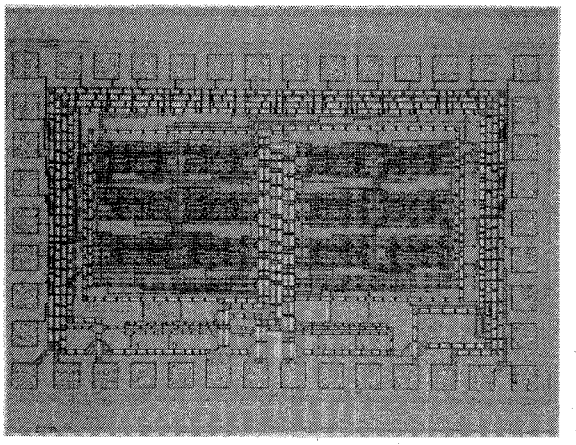


Fig. 10. Element control interface chip (ECI).

(SFDR) in MMIC form. It is based upon a 0.5 μm$\times$600 μm eight finger interdigitated HEMT device. The devices were fabricated on selectively doped AlGaAs/GaAs heterostructures grown by molecular beam epitaxy (MBE) on 50 mm diameter semi-insulating GaAs substrates. These HEMT's employ a large cross-section T-shaped plated gate and eight 75 μm long gate fingers in order to minimize gate resistance. The epitaxial material layer structure consists of a 300 Å GaAs cap layer Si doped to 5×10^{18} cm^{-3}, a 450 Å AlGaAs layer Si doped to 2×10^{18} cm^{-3}, a 40 Å undoped AlGaAs spacer, and a 1 μm undoped GaAs buffer layer. A 23% aluminum composition was used for the AlGaAs layers. Source inductive feedback is employed in both stages to bring input VSWR match into coincidence with input noise figure match. Shunt R-L feedback in the second stage is utilized for flat gain and good output VSWR match. The amplifier was fabricated at the General Electric Electronics Laboratory using a hybrid process consisting of optical stepper projection lithography with *E*-beam defined gates. Chip size measures 3.9 mm$\times$1.6 mm. Typical performance versus frequency is 16 to 18 dB of gain from 3.0 to 6.0 GHz, noise figure is less than 2.4 dB, and averaging 1.8 dB within the band. Input return loss varies from 12.5 dB to 5 dB, while output return loss varies from 25 dB to 8 dB, across the band. Output third-order intercept point of the MMIC amplifier ranges from +25 dBm to +27 dBm, with a corresponding spur-free dynamic range of between 78.4 dB/MHz and 79 dB/MHz. The 1 dB gain compression point output power occurs at +16 dBm.

Interface

Fig. 10 is the element control interface chip which solves the problem of interfacing a complex module with a large number of discrete lines and unique drive level requirements to a digital controller. It is impractical from a mechanical viewpoint to traverse the only available interface region of the module (the back end, whose width is determined by array pitch), with ten to a hundred control and power signals. In addition, the higher the number of interface lines, the better the potential for undesirable interference coupling from the digital beamsteering controller circuits. The ECI, shown in block diagram form in Fig. 11, functions as a serial-in/parallel-out shift-register/latch/driver, accepting serial TTL digital data input, providing appropriate voltage level outputs, and synchronized timing for T/R module mode switching. The ECI implemented in Tri-Quint enhancement/depletion digital GaAs using low power Buffered FET Logic provides these basic functions with output levels of 0 V and −3 V that are appropriate for the Harris 0.5 μm G-10 process. The ECI is capable of switching and settling the worst case capacitive load of the VGA at 15 pF in less than 100 ns. Clock rate is specified as 25 MHz, and chip size is 2.3 mm$\times$1.0 mm.

Module Construction

Fig. 12 is a photograph of the wideband *S*/*C*-band T/R module. Although the measured performance includes the circulator, it is not shown in this photograph as it is located at the next level of assembly within the antenna system which integrates the beamsteering controller (BSC) with the T/R module. The T/R module package is a low parasitic, hermetic structure composed of base, ceramic mother substrate, ceramic wall, and lid. The base is molybdenum, which provides a good thermal interface and possesses a coefficient of thermal expansion compatible with both Alumina and GaAs. The mother substrate incorporates all RF circuitry on the top surface with thin film TaN resistors for voltage conditioning/50 Ω terminations and thick film multi-layer dc and control distribution on the backside. A full thick film plane has been devoted to HPA voltage distribution. Backside thick film ground planes minimize coupling and provide the reference ground plane for the frontside microstrip circuitry. Laser-tooled vias filled with thick film gold provide the connection to the top surface and cut-outs are provided for the MMIC chips. Spacers are utilized to maintain planarity. The ceramic mother substrate is sealed to the ceramic wall with low-temperature glass. Prior to integration of the power amplifiers, the mother substrate/frame combination is soldered to the base. The

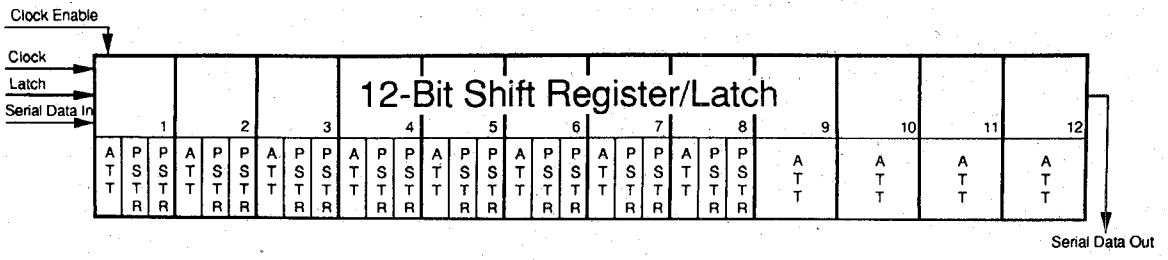


Fig. 11. Block diagram of ECI.

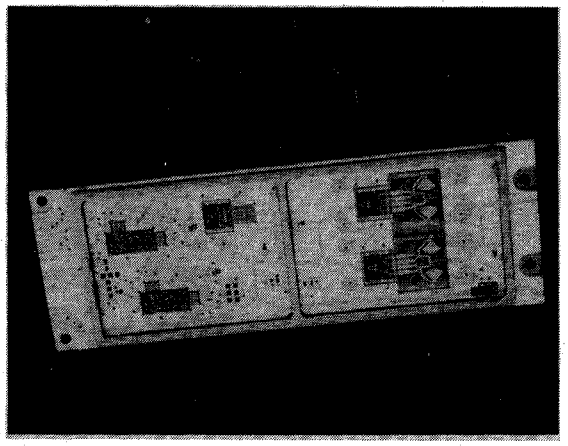


Fig. 12. Wideband S/C-band T/R module.

power amplifiers are then eutectically bonded into the package. RF tested small-signal devices are epoxied into the package. A machined metal lid with recessed cavities for inclusion of microwave absorber is incorporated to decrease the possibility of moding and enhance module stability since the gross small-signal gain of the module totals 50 to 60 dB. Module size including the circulator and lid is 4.4 in $\times$ 1.16 in $\times$ 0.5 in, which is compatible with the grid spacing required for grating lobe free operation over a $\pm 45°$ azimuth/$\pm 60°$ elevation scan angle.

Measured Performance

Transmit and receive performance of a typical S/C-band T/R module is summarized in Table I. Six modules of this configuration were assembled, and reworked as necessary to achieve functionality. Since all the MMIC's utilized were from four lots of one to four wafers, performance was similar, and the sample size is statistically insignificant to draw any conclusions about module-to-module performance.

The measured performance in Table I is summarized in minimum, maximum, and rms over the 3.0 to 6.0 GHz frequency band. In addition, peak and rms performance is summarized over gain and phase states. These module level performance figures include all circuitry and the external circulator. Further detail plots as a function of frequency of receive gain for all 256 gain states, receive phase for all 256 phase states, noise figure, power output, and IMD versus input power are given in reference [8]. Peak performance within the 3.0 to 6.0 GHz band includes a power output of 21 W at S-band and 19 at C-band, a noise figure of 3.9 to 5.0 dB, 30 to 38 dB of receive gain, 40 dB of gain control in 256 steps and a +25 to +26 dBm output third order intercept point. IMD products are −55.9 dBc for a −35 dBm input at each tone at 4.4 GHz. Across a 30 dB receive gain adjustment range, the incidental phase shift is less than 8.9 degrees RMS, and below 3 degrees rms across 90% of the 3.0 to 6.0 GHz band. Calibrated rms phase error is less than 1 degree with less than 1.2 dB RMS amplitude variation. The worst case match at the beamformer port was 2.3:1, while at the antenna port, worst case was 3:1. Over 70% of the band, both ports are better than 1.5:1. The module requires 5.5 V at 600 mA and −3.5 V at 160 mA in receive and an additional 9 V at 16 A during transmit in Class A operation. It is of note that due to the module architecture, both noise figure and IMD response degrade slowly with gain setting as shown in Tables II and III. Although the second stage contribution to noise figure is significant as described below, by positioning the variable gain amplifier last, the second stage noise figure

TABLE I
Performance Summary of S/C-Band T/R Module (3.0 to 6.0 GHz Frequency Band)

Parameter	Min	Max	RMS
Receive gain (dB)	25	38	30.9
Gain range (dB)	37	42	39.5
Min gain resolution (dB)	0.03	0.04	0.035
Max gain resolution (dB)	2.9	4.6	4.1
Peak phase versus gain (°)	2.5	18	8.6
RMS phase versus gain (°)	0.3	8.9	3.3
Peak phase error (°)	0.6	4.5	3.7
RMS phase error (°)	0.9	1.0	0.95
Peak gain versus phase (dB)	0.6	3.5	1.6
RMS gain versus phase (dB)	0.4	1.2	0.74
VSWR-beamformer port	1.2	2.3	1.5
VSWR-antenna port	1.4	3.0	1.8
Noise figure (dB)	3.9	7.2	4.9
Output IP_3 (dBm)	25	26	25.5
Transmit gain (dB)	33	46	38
Output power (W)	8	21	16
Power-added efficiency (%)	5.8	14.2	10.8

TABLE II
Noise Figure Versus Gain at 3.2 GHz

VGA State	G (dB)	NF (dB)
255	36.5	3.99
32	20.8	4.09
16	16.1	4.26
8	9.5	4.90

TABLE III
IMD VERSUS GAIN AT 4.4 GHz (−35 dBm EACH TONE)

VGA State	G (dB)	IMD (dBc)
255	32.4	55.9
128	27.7	53.0
64	23.2	52.3
32	16.8	49.3
16	12.0	48.2

TABLE IV
GAIN/PHASE VERSUS TEMPERATURE/VOLTAGE

Gain versus temperature	0.09 db/°C
Phase versus temperature	0.16 deg/°C
Gain versus VDD	1.6 dB/V
Gain versus VSS	2.2 dB/V

is almost invariant to VGA setting until shared leg gain is reduced below 10 dB. Similarly, because most of the gain is distributed at the back-end of the shared leg, the IMD determining element is the VGA. Segmented dual gate VGA's reduce output power capability 3 dB for every major bit transition of gain control. Hence IMD degrades gradually until gain is reduced to the point that previous stages contribute significantly. Likewise, due to the module architecture and the selected circuit topologies which were optimized for insensitivity, the gain and phase variation of the module to temperature and voltage given in Table IV is quite small.

PERFORMANCE ENHANCEMENT

This achievement can be attributed to accurate device models, a comprehensive design methodology, robust matching circuit topologies, and high yield processing as documented in the [3]–[5], [7], [9]. With improvement to module design in the areas of isolation, shielding, and grounding, enhanced smoothness of frequency response has been realized in an iteration of this design. Advances in device technology will also yield improvements in performance. For example, the low noise amplifier shown in Fig. 9, has been reprocessed using a pseudomorphic HEMT layer structure. The results shown in Fig. 13 are outstanding with an improved gain of 23 dB, and noise figure of less than 2.0 dB, reaching 1.5 dB at midband. The present module noise figure response is composed of the elements in front of the LNA, Trak 59A6201 circulator (0.6 dB), package insertion loss (0.1 dB), Alpha CLA3134 limiter diode/dc return (0.5 dB), LNA noise figure, and a large second-stage contribution due the gain of the conventional HEMT LNA and the dual channel receive signal split (the second stage noise figure of the Lange coupler/shared leg is 14 to 16 dB). The PHEMT MMIC LNA, incorporated into the iterated module design, has yielded a 3.0 dB module level noise figure. Similarly, a power device with improved structure will dramatically improve power-added efficiency. Although the Harris Microwave Semiconductor 0.5 μm MESFET foundry is high yield and versatile, the efficiency performance as a power amplifier is limited by use of a single

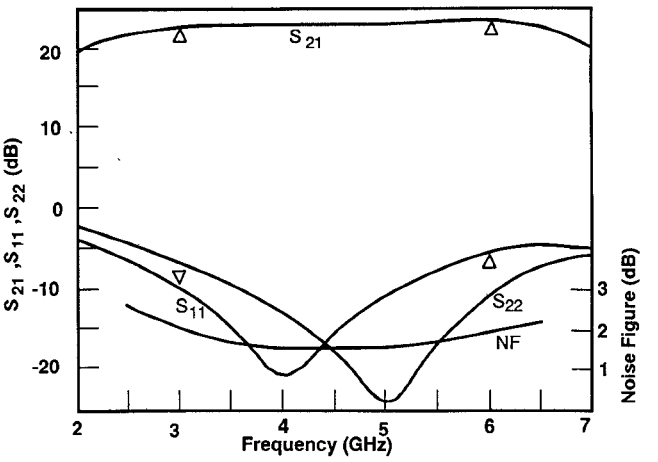


Fig. 13. Gain/noise figure/return loss of PHEMT SCLNA2.

implant. A p-type beryllium co-implant beneath the channel yields better electron confinement and a sharper pinch-off. The result is more constant transconductance, higher gain, improved power density and efficiency. A two stage driver amplifier, equivalent to that shown in Fig. 8, using an improved 0.5 μm MESFET based on this technology has been fabricated at the General Electric Electronics Laboratory. It has achieved 4 W at 36% power-added efficiency.

PERFORMANCE COMPARISON

The measured performance described herein is based upon first pass MMIC and first pass module design and fabrication, and includes circulator, packaging, digital interface, and power conditioning losses. Although the literature is scarce as to module level performance, what has been published at the module level [10]–[12] is eclipsed by orders of magnitude in every parameter by these results.

CONCLUSION

A complex wideband transmit/receive module has achieved performance levels superior to any MMIC module. The module incorporates a compact digital interface, requires only three supply voltages, and utilizes advance packaging techniques, resulting in a size compatible with a grating lobe free grid spacing.

ACKNOWLEDGMENT

The authors would like to acknowledge the many individuals at General Electric who contributed to the design, fabrication, and processing of the described circuits. In particular, A. Jacomb-Hood, C. Grondahl, and T. Cokinos for chip design, E. Lewis for MMIC layout, W. Kong for HEMT processing, C. Low, A. Sun, and M. Katz for module fabrication, A Thatcher for assembly, R. Clark and S. Miller for module engineering, and H. Marcus for mechanical design. We would also like to acknowledge the contributions of Harris Microwave Semiconductor and Tri-Quint Semiconductor for foundry service.

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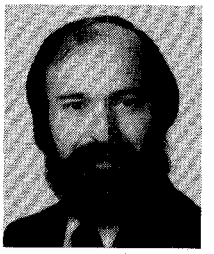

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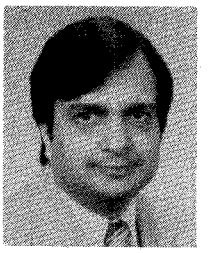

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